Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A processor, comprising:

decode logic adapted to decode system commands and instructions in a first mode and in a second mode, wherein the first mode corresponds to a first instruction set and the second mode corresponds to a second instruction set, and wherein the system commands are accessible in either mode through a common Bytecode.

2 (Original) The processor of claim 1, wherein the system commands belong to the first instruction set.

3. (Original) The processor of claim 1, wherein the system commands belong to the second instruction set.

4. (Original) The processor of claim 1, wherein the common Bytecode corresponds to a predetermined prefix, wherein the first and second instruction set each comprises the predetermined prefix.

5. (Original) The processor of claim 4, wherein the predetermined prefix is a Java Impdep2 Bytecode.

6. (Currently Amended) The processor of claim 4, wherein the processor further comprises a pre-decode logic coupled to the decode logic, and wherein the pre-decode logic is adapted to pre-decode the predetermined prefix concurrently with the decode logic decoding a preceding instruction.

7. (Original) The processor of claim 4, wherein the predetermined prefix indicates that a system command follows.

8. (Original) The processor of claim 4 wherein the predetermined prefix is decoded.

9. (Currently Amended) A method, comprising:

decoding instructions from one instruction set in a current mode;

detecting a predetermined prefix indicating a succeeding instruction is a system command;

refraining from decoding the predetermined prefix; and

decoding the system command when executing ~~instruction~~ instructions in the current mode.

10. (Original) The method of claim 9, wherein the predetermined prefix is a Java Impdep2 Bytecode.

11. (Original) The method of claim 9, wherein the one instruction set and another instruction set each comprises the Java Impdep2 Bytecode.

12. (Original) The method of claim 11, wherein the system commands belong to either one instruction set or another instruction set.

13. (Original) The method of claim 9, wherein the step of decoding instructions from one instruction set and the step of detecting a predetermined prefix occur concurrently.

14. (Original) The method of claim 9, wherein the step of decoding instructions from one instruction set and the step of detecting a predetermined prefix occur sequentially.

15. (Original) The method of claim 14, wherein the step of decoding instructions from one instruction set and the step of detecting a predetermined prefix occur sequentially further comprises decoding the predetermined prefix.

16. (Original) A processor, comprising:

decode logic adapted to decode instructions from a first instruction set in a first mode and decode instructions from a second instruction set in a second mode;

pre-decode logic coupled to the decode logic, wherein the pre-decode logic is adapted to pre-decode instructions prior to loading the instruction into the decode logic; and

wherein while the decode logic is decoding an instruction from the first instruction set or a second instruction set, the pre-decode logic detects a predetermined prefix indicating a succeeding instruction is a system command, the decode logic remains in a current mode and decodes the succeeding instruction.

17. (Original) The processor of claim 16, wherein the decode logic is decoding instructions from the first instruction set, and wherein the current mode is the first mode.

18. (Original) The processor of claim 16, wherein the decode logic is decoding instructions from the second instruction set, and wherein the current mode is the second mode.

19. (Original) The processor of claim 16, wherein the predetermined prefix is a Java Impdep2 Bytecode, and wherein the first and second instruction set each comprises the Java Impdep2 Bytecode.

20. (Original) The processor of claim 16, wherein the decode logic skips decoding of the predetermined prefix and decodes the succeeding instruction immediately following the instruction from the first instruction set.

21. (Original) The processor of claim 16, wherein the decode logic decodes the predetermined prefix immediately following the instruction from the first instruction set.

22. (Original) The processor of claim 16, wherein the system command belongs to the first instruction set.

23. (Original) The processor of claim 16, wherein the system command belongs to the second instruction set.

24. (Currently Amended) A system, comprising:

main processor;

co-processor coupled to the main processor, the co-processor comprising:

decode logic adapted to decode instructions from a first instruction set in a first mode and decode instructions from a second instruction set in a second mode; and

wherein upon detecting a predetermined prefix indicating a succeeding instruction is a system command, the co-processor stays ~~stay~~ in the current mode.

25. (Original) The system of claim 24, wherein the current mode is the first mode, and wherein the system command belongs to the first or second instruction set.

26. (Original) The system of claim 24 wherein the predetermined prefix is a Java Impdep2 Bytecode, and wherein the first and second instruction sets each comprises the Java Impdep2 Bytecode.

27. (Original) The system of claim 24, wherein the co-processor further comprises a pre-decode logic coupled to the decode logic and wherein the pre-decode logic is adapted to detect the predetermined prefix.

28. (Original) The system of claim 27, wherein the pre-decode logic is further adapted to pre-decode the predetermined prefix concurrently with the decode logic decoding a previous instruction.

29. (Original) The system of claim 24, wherein the predetermined prefix is decoded sequentially after the decode logic decodes a previous instruction.

30. (Original) The system of claim 24, wherein the system comprises a cellular telephone.